What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory circuit comprising:

a data buffer coupled to a storage array of said memory circuit;

a logic circuit for receiving input data associated with a write command, said logic circuit being coupled to said data buffer and said storage array,

wherein when said input data associated with said write command is received by said logic circuit, said logic circuit in response to a first control signal sends said input data directly to said storage array or sends said input data to said data buffer.

2. The memory circuit according to claim 1, further comprising:

a command decoder coupled to said logic circuit, said command decoder providing said first control signal to said logic circuit.

3. The memory circuit according to claim 2, further comprising:

a controller coupled to said command decoder, said controller determining if said input data will be sent directly to said storage array or to said data buffer, said controller providing a second control signal to said command decoder, said command decoder in response to said second control signal providing said first

control signal to said logic circuit, said first control signal being based on said second control signal.

4. The memory circuit according to claim 2, wherein said command decoder is coupled to said data buffer, and if said input data is sent to said data buffer, said command decoder sends a third control signal to said data buffer at a predetermined time, said data buffer in response to said third control signal sending said input data from said data buffer to said storage array.

5. The memory circuit according to claim 4, wherein said predetermined time is a time when input/output gates associated with said storage array are not being used.

6. The memory circuit according to claim 5, further comprising:

a second logic circuit coupled to said controller and said command decoder, said second logic circuit receiving an address associated with said input data from said controller;

an address buffer coupled to said second logic circuit; and

an address decoder coupled to said address buffer and said storage array,

wherein if said input data is sent to said data buffer, said second logic circuit in response to a fourth control signal from said command decoder sends said address to said address buffer, and said address buffer in response to a fifth control signal sent from said command decoder at said predetermined time sends said address to said

address decoder, said address decoder decoding said address and activating a portion of said storage array into which said data is written.

7. The memory circuit according to claim 6, wherein if said input data is sent directly to said storage array, said logic circuit in response to said fourth control signal sends said address to said address decoder.

8. The memory circuit according to claim 5, further comprising:

an address decoder coupled to said controller and said storage array, said address decoder receiving an address associated with said input data from said controller,

wherein if said input data is sent to said data buffer, said controller delays sending said address associated with said input data to said address decoder until said third control signal is sent to said data buffer.

9. The memory circuit according to claim 1, wherein said input data is sent directly to said storage array if said write command is followed by another write command.

10. The memory circuit according to claim 1, wherein said input data is sent to said data buffer if said write command is followed by a read command.

11. A memory device comprising:

an array of memory cells for storing data;

a data buffer coupled to said array; and

a logic circuit coupled to said data buffer and said array,

wherein when a write command to write input data to said array is received, said logic circuit, in response to a control signal, sends said input data associated with said write command directly to said array or sends said input data to said data buffer.

12. The memory device according to claim 11, further comprising:

a command decoder coupled to said logic circuit, said command decoder providing said control signal to said logic circuit.

13. The memory device according to claim 12 further comprising:

a controller coupled to said command decoder, said memory controller determining if said input data is to be sent from said logic circuit directly to said array or to said data buffer.

14. The memory device according to claim 13, wherein if said input data is to be sent to said data buffer, said controller sends a posted write signal to said command decoder, said command decoder in response to said posted write signal sending said control signal to said logic circuit, said control signal being based on said posted write signal.

15. The memory device according to claim 14, wherein said posted write signal is sent by said controller if said write command is followed by a read command.

16. The memory device according to claim 15, further comprising:

a second logic circuit coupled to said controller and said command decoder, said second logic circuit receiving an address associated with said input data from said controller;

an address buffer coupled to said second logic circuit; and

an address decoder coupled to said address buffer and said array,

wherein if said input data is sent to said data buffer, said logic circuit in response to a second control signal from said command decoder sends said address to said address buffer, and said address buffer in response to a third control signal sent from said command decoder sends said address to said address decoder, said address decoder decoding said address and activating a portion of said array into which said data is written.

17. The memory device according to claim 16, wherein if said input data is sent directly to said array, said second logic circuit in response to said second control signal sends said address to said address decoder.

18. The memory device according to claim 15, wherein said command decoder is coupled to said data buffer, and if said input data is sent to said data buffer, said data

buffer in response to a signal from said command decoder sends said input data to said array.

19. The memory device according to claim 18, further comprising:

an address decoder coupled to said controller and said array, said address decoder receiving an address associated with said input data from said controller,

wherein if said input data is sent to said data buffer, said controller delays sending said address associated with said input data to said address decoder until said signal is sent from said command decoder.

20. The memory device according to claim 18, wherein said signal from said command decoder is sent when input/output gates associated with said array are not being used.

21. The memory device according to claim 11, further comprising:

a latch coupled between said logic circuit and said array and coupled between said data buffer and said array, said input data being latched by said latch before being sent to said array from said logic circuit or said data buffer.

22. The memory device according to claim 21, further comprising:

a plurality of input/output gates coupled between said array and said latch.

23. The memory device according to claim 11, wherein said input data is sent directly to said array if said write command is followed by another write command.

24. The memory device according to claim 11, wherein said input data is sent to said data buffer if said write command is followed by a read command.

25. A memory system comprising:

a storage array for storing data, said data being input to said storage array in response to a write command and said data being extracted from said storage array in response to a read command; and

a data buffer coupled to said storage array, said data buffer adapted to store input data associated with a write command;

wherein said memory system includes circuitry for determining on a per command basis if input data associated with a write command is posted in said data buffer before being sent to said storage array.

26. The memory system according to claim 25, wherein said input data associated with said write command will be posted in said data buffer if a read command follows said write command.

27. The memory system according to claim 26, wherein said input data posted in said buffer is sent to said storage array when output data associated with said read command is being output from said memory system.

28. The memory system according to claim 27, further comprising:

an address buffer coupled to said storage array, wherein an address associated with said input data posted in said buffer is stored in said address buffer until said input data posted in said buffer is sent to said storage array.

29. The memory system according to claim 27, further comprising:

a controller coupled to said storage array, said controller providing an address associated with said input data to said storage array, wherein said controller delays sending said address associated with said input data posted in said buffer until said input data posted in said buffer is sent to said storage array.

30. The memory system according to claim 25, wherein said input data associated with said write command is not posted in said data buffer if another write command follows said write command.

31. The memory system according to claim 25, wherein said circuitry further comprises:

a logic circuit coupled to said storage array and said data buffer,

wherein said logic circuit, in response to a control signal, sends said input data associated with said write command to be posted in said data buffer before being sent to said storage array or to said storage array without being posted in said data buffer.

32. A processing system comprising:

a processing unit; and

a memory device connected to said processing unit, said memory device comprising:

an array of memory cells for storing data;

a data buffer coupled to said array; and

a logic circuit coupled to said data buffer and said array,

wherein when a write command to write input data to said array is issued by said processing unit, said logic circuit, in response to a control signal, sends said input data associated with said write command directly to said array or sends said input data to said data buffer.

33. The processing system according to claim 32, wherein said memory device further comprises:

a command decoder coupled to said logic circuit, said command decoder providing said control signal to said logic circuit.

34. The processing system according to claim 33, further comprising:

a controller coupled to said command decoder, said memory controller determining if said input data is to be sent from said logic circuit directly to said array or to said data buffer.

35. The processing system according to claim 34, wherein if said input data is to be sent to said data buffer, said controller sends a posted write signal to said command decoder, said command decoder in response to said posted write signal sending said control signal to said logic circuit, said control signal being based on said posted write signal.

36. The processing system according to claim 35, wherein said posted write signal is sent by said controller if said write command is followed by a read command.

37. The processing system according to claim 36, further comprising:

a second logic circuit coupled to said controller and said command decoder, said second logic circuit receiving an address associated with said input data from said controller;

an address buffer coupled to said second logic circuit; and

an address decoder coupled to said address buffer and said array,

wherein if said input data is sent to said data buffer, said logic circuit in response to a second control signal from said command decoder sends said address to said address buffer, and said address buffer in response to a third control signal sent

from said command decoder sends said address to said address decoder, said address decoder decoding said address and activating a portion of said array into which said data is written.

38. The processing system according to claim 37, wherein if said input data is sent directly to said array, said second logic circuit in response to said second control signal sends said address to said address decoder.

39. The processing system according to claim 33, wherein said command decoder is coupled to said data buffer, and if said input data is sent to said data buffer, said data buffer in response to a signal from said command decoder sends said input data to said array.

40. The processing system according to claim 39, further comprising:

an address decoder coupled to said controller and said array, said address decoder receiving an address associated with said input data from said controller,

wherein if said input data is sent to said data buffer, said controller delays sending said address associated with said input data to said address decoder until said signal is sent from said command decoder.

41. The processing system according to claim 39, wherein said signal from said command decoder is sent when input/output gates associated with said array are not being used.

42. The processing system according to claim 32, wherein said memory device further comprises:

a latch coupled between said logic circuit and said array and coupled between said data buffer and said array, said input data being latched by said latch before being sent to said array from said logic circuit or said data buffer.

43. The processing system according to claim 42, wherein said memory device further comprises:

a plurality of input/output gates coupled between said array and said latch.

44. The processing system according to claim 32, wherein said input data is sent directly to said array if said write command is followed by another write command.

45. The processing system according to claim 32, wherein said input data is sent to said data buffer if said write command is followed by a read command.

46. The processing system according to claim 32, wherein said processing unit and said memory device are integrated on a single chip.

47. A processing system comprising:

a processing unit; and

a memory system connected to said processing unit, said memory system comprising:

a storage array for storing data, said data being input to said storage array in response to a write command and said data being extracted from said storage array in response to a read command; and

a data buffer coupled to said storage array, said data buffer adapted to store input data associated with a write command;

wherein said memory system includes circuitry for determining on a per command basis if input data associated with a write command is posted in said data buffer before being sent to said storage array.

48. The processing system according to claim 47, wherein said input data associated with said write command will be posted in said data buffer if a read command follows said write command.

49. The processing system according to claim 48, wherein said input data posted in said buffer is sent to said storage array when output data associated with said read command is being output from said memory system.

50. The processing system according to claim 49, further comprising:

an address buffer coupled to said storage array, wherein an address associated with said input data posted in said buffer is stored in said address buffer until said input data posted in said buffer is sent to said storage array.

51. The memory system according to claim 49, further comprising:

a controller coupled to said storage array, said controller providing an address associated with said input data to said storage array, wherein said controller delays sending said address associated with said input data posted in said buffer until said input data posted in said buffer is sent to said storage array.

52. The processing system according to claim 47, wherein said input data associated with said write command is not posted in said data buffer if another write command follows said write command.

53. The processing system according to claim 47, wherein said circuitry of said memory system further comprises:

a logic circuit coupled to said storage array and said data buffer,

wherein said logic circuit, in response to a control signal, sends said input data associated with said write command to be posted in said data buffer before being sent to said storage array or to said storage array without being posted in said data buffer.

54. The processing system according to claim 47, wherein said processing unit and said memory system are integrated on a single chip.

55. A method for writing input data associated with a write command into an array, said method comprising the steps of:

receiving said input data associated with said write command;

receiving a first control signal indicating said input data associated with said write command should be posted;

posting said input data associated with said write command in response to said first control signal;

receiving a second control signal indicating said input data associated with said write command should not be posted; and

sending said input data to said array without posting said input data in response to said second control signal.

56. The method according to claim 55, further comprising:

determining a next command following said write command.

57. The method according to claim 56, wherein if said next command following said write command is another write command, said method further comprises:

providing said second control signal and sending said input data to said array without posting said input data.

58. The method according to claim 56, wherein if said next command following said write command is a read command, said method further comprises:

providing said first control signal and posting said input data associated with said write command.

59. The method according to claim 58, wherein said step of posting further comprises:

sending said input data associated with said write command to a data buffer; and

storing said input data associated with said write command in said data buffer.

60. The method according to claim 59, further comprising:

determining a time period when input/output gates associated with said array are not being used; and

sending said input data associated with said write command stored in said data buffer to said array during said time period.

61. The method according to claim 60, further comprising:

storing an address associated with said input data in an address buffer; and

sending said address to said array when said input data associated with said write command stored in said data buffer is sent to said array.

62. The method according to claim 60, further comprising:

storing an address associated with said input data in a controller; and

delaying sending said address from said controller to said array until said input data associated with said write command stored in said data buffer is sent to said array.

63. The method according to claim 60, wherein said step of sending said input data associated with said write command stored in said data buffer to said array further comprises:

latching said input data associated with said write command in a latch.

64. The method according to claim 63, wherein said step of sending said input data associated with said write command stored in said data buffer to said array further comprises:

sending said latched input data to a gate associated with said array; and

writing said input data into said array from said gate.

65. The method according to claim 55, wherein said step of sending said input data associated with said write command to said array further comprises:

latching said input data associated with said write command in a latch.

66. The method according to claim 65, wherein said step of sending said input data associated with said write command to said array further comprises:

sending said latched input data to a gate associated with said array; and

writing said input data into said array from said gate.

67. A method for posting input data associated with a write command, said method comprising the steps of:

determining a next command following said write command; and

if said next command is a read command, posting said input data associated with said write command, otherwise not posting said input data associated with said write command.

68. The method according to claim 67, wherein said step of posting further comprises:

sending said input data associated with said write command to a data buffer; and

storing said input data associated with said write command in said data buffer.

69. The method according to claim 68, further comprising:

determining a time period when input/output gates associated with a memory array are not being used; and

sending said input data associated with said write command stored in said data buffer to said memory array during said time period.

70. The method according to claim 69, further comprising:

storing an address associated with said input data in an address buffer; and

sending said address to said array when said input data associated with said write command stored in said data buffer is sent to said memory array.

71. The method according to claim 69, further comprising:

storing an address associated with said input data in a controller; and

delaying sending said address from said controller to said memory array until said input data associated with said write command stored in said data buffer is sent to said memory array.